Amendments to the Claims

1. (Currently Amended) A PHY (Physical Layer) to provide data to a MAC (Media Access Control) via PHY-to-MAC words and to receive data and commands from the MAC via MAC-to-PHY words, the PHY comprising:

at least one PHY-to-MAC port to provide signals indicative of the PHY-to-MAC words;

at least one MAC-to-PHY port to receive signals indicative of the MAC-to-PHY words; and

a register to store a pointer to a memory location so as to provide identification information about the PHY-; and

at least one Reset/Sync port to receive a signal to provide synchronization so that the PHY-to-MAC words and MAC-to-PHY words are synchronized into pairs, wherein a pair comprises one MAC-to-PHY word and one PHY-to-MAC word.

2. (Cancelled)

3. (Currently Amended) A MAC (Media Access Control) to provide data and commands to a PHY (Physical layer) via MAC-to-PHY words and to receive data from the PHY via PHY-to-MAC words, the MAC comprising:

at least one MAC-to-PHY port to provide signals indicative of the MAC-to-PHY words;



at least one PHY-to-MAC port to receive signals indicative of the PHY-to-MAC words; wherein the at least one PHY-to-MAC port receives a signal indicative of a pointer to a memory location so as to provide identification information about the PHY-; and

at least one Reset/Sync port to provide a signal to synchronize the PHY-to-MAC words and MAC-to-PHY words into pairs, wherein a pair comprises one MAC-to-PHY word and one PHY-to-MAC word.

4. (Cancelled)

5. (Currently Amended) A chipset comprising:

a MAC (Media Access Control) to provide data and commands to a PHY

(Physical layer) via MAC-to-PHY words and to receive data from the PHY via PHY-toMAC words, wherein the MAC comprises:

at least one MAC-to-PHY port to provide signals indicative of the MAC-to-PHY words; and

at least one PHY-to-MAC port to receive signals indicative of the PHY-to-MAC words; wherein the at least one PHY-to-MAC port receives a signal indicative of a pointer to a memory location so as to provide identification information about the PHY-; and

at least one Reset/Sync port to provide a signal to synchronize the PHY-to-MAC words and MAC-to-PHY words into pairs, wherein a pair comprises one MAC-to-PHY word and one PHY-to-MAC word.

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6. (Cancelled)

- 7. The chipset as set forth in claim 5 further comprising a register, wherein the chipset loads the identification information into the register.
- 8. (Cancelled)
- 9. (Currently Amended) A computer system comprising:
 - a first memory device;
 - a MAC (Media Access Control);
- a PHY (Physical layer) to provide data to the MAC via PHY-to-MAC words and to receive data and commands from the MAC via MAC-to-PHY words, the PHY comprising:
- at least one PHY-to-MAC port to provide signals indicative of the PHY-to-MAC words;
- at least one MAC-to-PHY port to receive signals indicative of the MAC-to-PHY words; and
- a register to store a pointer to a memory location in the first memory device so as to provide identification information about the PHY.
- wherein the PHY-to-MAC words and the MAC-to-PHY words are synchronized into pairs, where a pair comprises one PHY-to-MAC word and one MAC-to-PHY word.

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- The computer system as set forth in claim 9, wherein the MAC further comprises a register to store the identification information.
- 11. The computer system as set forth in claim 9, further comprising:

a processor;

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system memory;

secondary memory to store a device driver for the PHY; wherein the processor loads the device driver from the secondary memory into system memory based upon the identification information.

- 12. The computer system as set forth in claim 11, wherein the MAC further comprises a register to store the identification information.
- 13. (Currently Amended) The computer system as set forth in claim 11, further comprising a second memory device to store BIOS (Basic Input Output System), wherein the processor loads the device driver independently of loading the BIOS.
- 14. The computer system as set forth in claim 12, further comprising a second memory device to store BIOS, wherein the processor loads the device driver independently of loading the BIOS.
- 15. The computer system as set forth in claim 14, further comprising: a system bus; and



a chipset in communication with the system bus, wherein the MAC is integrated with the chipset.